What is claimed is:

1. An apparatus for testing a semiconductor integrated circuit comprising:

a test circuit board for exchanging signals with a semiconductor integrated circuit under test; and

an ancillary test device which is disposed in the vicinity of the test circuit board and connected to the test circuit board;

wherein the ancillary test device comprises digital circuit testing capability for testing a digital circuit included in the semiconductor integrated circuit under test;

the ancillary test device comprises test pattern memory for storing a plurality of test pattern data sets corresponding to a plurality of test items for testing the digital circuit, a test pattern signal generator into which are written test pattern data selected from a plurality of test pattern data sets stored in the test pattern memory, and a control section for controlling an operation for the test pattern data selected from among the plurality of test pattern data sets stored in the test pattern memory and an operation for writing the selected test pattern data into the test pattern signal generator; and

the ancillary test device generates a test input pattern signal for the semiconductor integrated circuit under test on the basis of test pattern data written in the test pattern signal generator and determines a test output pattern signal output from the semiconductor integrated circuit under test on the basis of the test input pattern signal, thereby testing a digital circuit of the semiconductor integrated circuit under test.

2. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the test pattern memory is formed so as to have storage capacity greater than the storage capacity of the

test pattern signal generator.

3. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the ancillary test device further comprises a CPU section, the CPU section generates a selection instruction signal to be used for reading test pattern selected from the plurality of test pattern data sets stored in the test pattern memory, and the control section reads the test pattern data selected from the plurality of test pattern data sets stored in the test pattern memory in accordance with the selection instruction signal and writes the test pattern data into the test pattern signal generator.

4. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the control section reads the test pattern data written into the test pattern signal generator; and

the test pattern signal generator generates a test pattern signal and a test input/determination pattern signal on the basis of the read test pattern data.

5. The apparatus for testing a semiconductor integrated circuit according to claim 4, wherein the ancillary test device further comprises a waveform shaping section, the waveform shaping section shapes the test input pattern signal on the basis of the test pattern signal, and the test input pattern signal is input to the semiconductor integrated circuit under test.

6. The apparatus for testing a semiconductor integrated circuit according to claim 5, wherein the ancillary test device further comprises an output determination section, and the output determination section compares a test output pattern signal output from the semiconductor integrated circuit under test with the test pattern signal, thereby outputting an error data signal.

7. The apparatus for testing a semiconductor integrated circuit according to claim 6, wherein the ancillary test device further comprises an error information memory section, and the error information memory section is formed so as to receive address information to be used for reading the test pattern data written into the test pattern signal generator and also stores address information obtained when the output determination section has generated the error data signal.

8. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the test device comprises a test head device disposed in the vicinity of the test circuit board;

the test head device comprises an ancillary test assembly formed by combination of a plurality of circuit boards; and

the ancillary test device comprises circuit components mounted on the plurality of circuit boards in a distributed manner.

9. The apparatus for testing a semiconductor integrated circuit according to claim 8, wherein the ancillary test device assembly comprises five circuit boards;

two of the five circuit boards are arranged in substantially parallel with the test circuit board; and

the remaining three circuit boards are arranged substantially perpendicular to the test circuit boards.

10. The apparatus for testing a semiconductor integrated circuit according to claim 9, wherein the test head device comprises a test head having a scope hole; and

portions of the three circuit boards disposed substantially perpendicular to the test circuit board are arranged uniformly within the scope hole.

11. The apparatus for testing a semiconductor integrated circuit according to claim 2, wherein

the test pattern signal generator is constituted of memory which is higher in speed than the test pattern memory;

the test pattern signal generator stores a test vector address control code, test vector address control data, and test pattern data along a test vector address;

the control section comprises a program counter which generates a test vector address signal on the basis of the test vector address control code and test vector address control data; and

the test pattern signal generator generates a test pattern signal on the basis of the test pattern data while advancing the test vector address by means of the test vector address signal.

12. The apparatus for testing a semiconductor integrated circuit according to claim 2, wherein

the test pattern signal generator is constituted of memory which is higher in speed than the test pattern memory;

the test pattern signal generator stores, along test vector addresses, a control code for an algorithmic data generation register, control data for the algorithmic data generation register, a test vector address control code, and test vector address control data;

the control section comprises a program counter for generating a test vector address signal on the basis of the test vector address control code and test vector address control data, and a plurality of groups of registers for generating an algorithmic test pattern signal on the basis of the control code for an algorithmic data generation register and the control data for an algorithmic data generation register.

13. The apparatus for testing a semiconductor integrated

circuit according to claim 1, wherein the test pattern signal generator comprises a plurality of channels and is formed so as to read test pattern data from each of the channels;

the control section comprises a parallel-to-serial converter into which the test pattern data read from the channels are input; and

the parallel-to-serial converter comprises the function of serially outputting the test pattern data read from the respective channels for each test cycle.

14. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the ancillary test device further comprises a timing signal generator;

the timing signal generator has a test cycle signal, a set clock signal, a reset clock signal, and a strobe signal;

the set clock signal, the reset clock signal, and the strobe signal are generated respectively from the test cycle signal with a certain variable time delay;

the set clock signal is used for setting a timing at which the test input pattern signal rises;

the reset clock signal is used for setting a timing at which the test input pattern signal falls; and

the strobe signal is used for setting a timing at which there is determined a test output pattern output from the semiconductor integrated circuit under test on the basis of the test input pattern.

15. The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the ancillary test device further comprises an interface circuit which interfaces with the semiconductor integrated circuit under test, and an output determination section;

the interface circuit comprises a high-level voltage generator and a low-level voltage generator;

a high-level voltage output from the high-level voltage generator and a low-level voltage output from the low-level voltage generator are made variable;

the test input pattern is generated through use of the high-level voltage and the low-level voltage; and

the output determination section is formed so as to determine the level of the test output pattern signal output from the semiconductor integrated circuit under test through use of a high-level voltage for determination output from a high-level voltage generator for determination purpose and generates an error data signal pertaining to a high-level voltage of the test output pattern, an error data signal pertaining to a low-level voltage of the test output pattern signal, and an error data signal pertaining to a voltage between the high-level voltage and the low-level voltage.

16. An apparatus for testing a semiconductor integrated circuit comprising:

a test circuit board for exchanging signals with a semiconductor integrated circuit under test; and

an ancillary test device which is disposed in the vicinity of the test circuit board and connected to the test circuit board;

wherein the ancillary test device comprises digital circuit testing capability for testing a digital circuit included in the semiconductor integrated circuit under test;

the ancillary test device comprises test pattern memory for storing a plurality of test pattern data sets corresponding to a plurality of test items for testing the digital circuit, a test pattern signal generator into which are written test pattern data selected from a plurality of test pattern data sets stored in the test pattern memory, and a control section for controlling an operation for the test pattern data selected from among the plurality of test pattern data sets stored in the test pattern memory, an operation for writing

the selected test pattern data into the test pattern signal generator, and an operation for reading test pattern data from the test pattern signal generator;

the ancillary test device generates a test input pattern signal for the semiconductor integrated circuit under test on the basis of test pattern data read from the test pattern signal generator and determines a test output pattern signal output from the semiconductor integrated circuit under test on the basis of the test input pattern signal, thereby testing a digital circuit of the semiconductor integrated circuit under test;

the ancillary test device is formed from a plurality of circuit boards including a circuit board to which a storage medium is removably attached; and

the pattern data memory is formed from the storage medium.

17. An apparatus for testing a semiconductor integrated circuit comprising:

a test circuit board for exchanging signals with a semiconductor integrated circuit under test; and

an ancillary test device which is disposed in the vicinity of the test circuit board and connected to the test circuit board;

wherein the ancillary test device comprises digital circuit testing capability for testing a digital circuit included in the semiconductor integrated circuit under test;

the ancillary test device comprises test pattern memory for storing a plurality of test pattern data sets corresponding to a plurality of test items for testing the digital circuit, a test pattern signal generator having first and second memory devices into which are written test pattern data selected from a plurality of test pattern data sets stored in the test pattern memory, and a control section for controlling an operation for the test pattern data selected from among the plurality of test pattern data sets stored in the test pattern

memory, an operation for writing the selected test pattern data into the first and second memory devices of the test pattern signal generator, and an operation for reading test pattern data from the first and second memory devices of the test pattern signal generator;

the ancillary test device generates a test input pattern signal for the semiconductor integrated circuit under test on the basis of test pattern data read from the test pattern signal generator and determines a test output pattern signal output from the semiconductor integrated circuit under test on the basis of the test input pattern signal, thereby testing a digital circuit of the semiconductor integrated circuit under test; and

when first test pattern data written into the first memory of the test pattern signal generator are read, second test pattern data selected from the plurality of test pattern data sets stored in the test pattern memory are written into the second memory device.

18. The apparatus for testing a semiconductor integrated circuit according to claim 17, wherein the test pattern signal generator is formed from dual-port memory;

the first memory device is formed from a first port; and

the second memory is formed from a second port.

19. The apparatus for testing a semiconductor integrated circuit according to claim 17, wherein the test pattern signal generator is formed from first and second bank memory devices;

the first bank memory device constitutes the first memory; and

the second bank memory device constitutes the second memory.

20. A method of manufacturing a semiconductor integrated circuit comprising the step of testing the semiconductor integrated circuit; wherein

a test circuit board for exchanging signals with a semiconductor integrated circuit under test, and an ancillary test device which is disposed in the vicinity of the test circuit board and connected to the test circuit board are used in the step of testing the semiconductor integrated circuit;

the ancillary test device comprises digital circuit testing capability for testing a digital circuit included in the semiconductor integrated circuit under test;

the ancillary test device comprises test pattern memory for storing a plurality of test pattern data sets corresponding to a plurality of test items for testing the digital circuit, a test pattern signal generator into which are written test pattern data selected from a plurality of test pattern data sets stored in the test pattern memory, and a control section for controlling an operation for the test pattern data selected from among the plurality of test pattern data sets stored in the test pattern memory and an operation for writing the selected test pattern data into the test pattern signal generator; and

the ancillary test device generates a test input pattern signal for the semiconductor integrated circuit under test on the basis of test pattern data written in the test pattern signal generator and determines a test output pattern signal output from the semiconductor integrated circuit under test on the basis of the test input pattern signal, thereby testing a digital circuit of the semiconductor integrated circuit under test, in the step of testing the semiconductor integrated circuit.